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#### **Low Power Design in CMOS**

Digital Integrated Circuits Low Power Design © Prentice Hall 1995 Low Power Design in CMOS

#### **Jan Rabaey, «Low P**

The short circuit power, is caused by the direct path from the power supply to ground, during the transition phase where  $K$  is a constant that depends on the transistor sizes and the technology,  $V_t$  is the threshold voltage of the nMOS and pMOS transistors, is the rise or fall time of

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1) Hoi-Jun Yoo, Chris van Hoof: Integrated Circuits and Systems-Biomedical CMOS Springer, 2011 2) Jan Rabaey: Low Power Design Essentials (Integrated Circuits and Systems, Springer, 2 3) JBKuo, JHLou Low-voltage CMOS VLSI Circuits, Wiley, 1999 4) DC Reddy, Biomedical Signal Processing, Principles and Techniques, Tata McGraw 2005

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**Design of a Simple CMOS Bandgap Reference - IJENS**

[1] Robert A Pease, "The Design of Band-Gap Reference Circuits: Trials and Tribulations," IEEE Proc of the 1990 Bipolar Circuits and Technology Meeting, Minneapolis, Minnesota, Sept 1990 [2] K Lasanen, V Koorkala, "Design of A 1-V Low Power CMOS Bandgap Reference Based on ...

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• Jan Rabaey, Low Power Design Essentials, Springer 2009 • Michael Orshansky, Sani Nassif, Duane Boning, Design for Manufacturability and Statistical Design: A Constructive Approach, Springer 2008 • David Z Pan, Minsik Cho, Yuan Kun, Manufacturability Aware Routing in Nanometer VLSI (Foundations and Trends in Electronic Design Automation),

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